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(54) Semiconductor light emitting element driving circuit

Treiberschaltung für ein lichtemittierendes Halbleiterelement

Circuit d'attaque pour un élément photoémetteur à semi-conducteur

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Description

[0001] The present invention relates to a driving circuit for use as an LED driving circuit for displays, indicators, or LED printer heads, as a laser source driving circuit for optical disk apparatuses, exposure apparatuses for IC fabrication, or laser beam printers, or as a driving circuit for light emitting elements for optical communications.

[0002] Driving circuits for semiconductor light emitting elements represented by light emitting diodes (LEDs), and semiconductor lasers,are classified into two categories: a cathode common circuit and an anode common circuit.

[0003] In the cathode common circuit, the cathode of a light emitting element is connected to a low-potential reference voltage source, and its anode is connected to a constant current source.

[0004] In the anode common circuit, the anode of a light emitting element is connected to a high-potential reference voltage source, and its cathode is connected to a switching circuit and a constant current source.

[0005] One example of the former circuit is disclosed in Japanese Laid-Open Patent Application No. 2-296382. The latter circuit is expected as a future mainstream circuit since its switching speed is higher than that of the former.

[0006] Fig. 1 is a circuit diagram showing an example of a conventional semiconductor light emitting element driving circuit.

[0007] Referring to Fig. 1, this driving circuit consists of differentially connected bipolar transistors 1 and 2; a bipolar transistor 3 which operates with a constant current; a semiconductor light emitting element 4; a resistor 5; an inductance 6 of the line which connects the bipolar transistors for driving the semiconductor light emitting element and the semiconductor light emitting element; an inductance 7 of the line which connects the semiconductor light emitting element and a power supply; a junction capacitance 8 of the semiconductor light emitting element; collector-emitter capacitances 9 and 10 of the bipolar transistors 1 and 2, respectively; and a base-collector capacitance 11 of the bipolar transistor 3.

[0008] As in Fig. 1, in this semiconductor light emitting element driving circuit constituted by a conventional semiconductor integrated circuit, the emitters of the differentially connected bipolar transistors 1 and 2 are connected to the collector of the bipolar transistor 3 which has the same conductivity type and operates as a constant current source.

[0009] Unfortunately, in an arrangement such as this prior art shown in Fig. 1 the current waveform for driving a semiconductor light emitting element is in some instances significantly distorted.

[0010] Fig. 2 is a view for explaining the mechanism in which the driving current for the semiconductor light emitting element is distorted in the configuration illustrated in Fig. 1. This mechanism will be described below with reference to Fig. 2.

[0011] The semiconductor light emitting element 4 needs to be switched at a high speed with a constant current of about a few milliamperes to 100 milliamperes. Assume that the value of this constant current is I and the values of the inductances 6 and 7 are L_1 and L_2, respectively. Assuming the time during which the transistor 1 is activated from a cut-off state and the current flowing through the semiconductor light emitting element 4 reaches the constant current value I from substantially zero is t, counterelectromotive voltages V_1 and V_2 produced in the inductances 6 and 7, respectively, by this current change are

$$V_1 = L_1 \cdot I/t, \qquad V_2 = L_2 \cdot I/t$$

V_1 is transmitted to the base of the transistor 3 through the collector-emitter capacitance 9 of the transistor 1 and the base-collector capacitance 11 of the transistor 3. Likewise, V_2 is transmitted to the base of the transistor 3 through the junction capacitance 8 of the semiconductor light emitting element 4 and the capacitances 9 and 11.

[0012] The mutual conductance, g_m, of the bipolar transistors is expressed as follows:

$$g_m = \partial I_C/\partial V_{BE} = qI_C/kT$$

That is, a change in the potential applied to the base produces as a large change in the collector current. In this conventional arrangement, therefore, a potential variation occurring in the line inductance is transmitted to the base of the transistor 3 which operates with a constant current, thus distorting the collector current, i.e., the driving current waveform of the semiconductor light emitting element.

[0013] This distortion in the waveform is represented by overshoot or ringing. If overshoot takes place, a semiconductor light emitting element deteriorates, and this consequently reduces the life of a product using this semiconductor light emitting element.

[0014] Examples of techniques for preventing this include circuit configurations shown in Figs. 3 and 4. In Fig. 3, a snubber circuit consisting of a resistor 12 and a capacitor 13 is additionally provided externally to the package incorporating a semiconductor light emitting element driving circuit. In Fig. 4, the emitters that are differentially connected and the base and collector of the transistor which operates with constant current are extracted to terminals, and a coil 14 or a capacitor 24 is inserted to stabilise the constant current.

[0015] The technique illustrated in Fig.3, however, delays the rise time due to the resistor and the capacitor for removing overshoot, leading to a decrease in the driving frequency.

[0016] In the technique illustrated in Fig. 4, the

number of package pins and the number of parts are increased.

[0017] In Figs. 3 and 4, connecting terminals are denoted by 19, 20, 21 and 22.

[0018] A driving circuit having the features recited in the preamble of claim 1 appended hereto, is disclosed in each of United States Patents US-A-4,539,686 and US-A-4,709,370. In the former, a feedback controlled bias current source is coupled to the light emitting element, in parallel with the switching transistor of the differential pair of bipolar transistors, to cancel modulation current and thus eliminate current overshoot on switching.

[0019] The present invention is intended to realise a semiconductor light emitting element driving circuit capable of driving a semiconductor light emitting element with a stable driving current by eliminating distortion of the waveform of the driving current for the semiconductor light emitting element, thereby preventing deterioration of the semiconductor light emitting element and increasing the life of a product.

[0020] The driving circuit of the present invention is characterised in that the constant current source is formed of a plurality of MOS FET drive transistors which are connected in parallel and have their drains connected to the emitters of the bipolar transistors, each of the MOS FET transistors having, connected to its gate electrode, a respective time constant circuit consisting of a resistor and a capacitor.

[0021] In the accompanying drawings:

Fig. 1 is a circuit diagram showing a conventional semiconductor light emitting element driving circuit;
Fig. 2 is a view showing voltage waveforms and current waveforms at individual nodes when the circuit in Fig. 1 is in operation;
Fig. 3 is a circuit diagram showing another conventional driving circuit;
Fig. 4 is a circuit diagram showing still another conventional driving circuit;
Fig. 5 is a circuit diagram showing a semiconductor light emitting element driving circuit, a prototype of a preferred embodiment of the present invention;
Fig. 6 is a view for explaining voltage waveforms and current waveforms at individual nodes when the circuit in Fig. 5 is in operation;
Figs. 7A to 7C are views showing semiconductor light emitting element driving current waveforms and constant current NMOS gate voltage waveforms;
Fig. 8 is a circuit diagram showing a driving circuit according to a preferred embodiment of the present invention;
Fig. 9 is a sectional view showing a portion of a driving circuit chip to implement the preferred embodiment;
Fig. 10 is a sectional view showing another portion of the driving circuit chip of Fig. 9; and
Figs. 11A and 11B are schematic views showing the arrangements of systems in which the driving circuit of the present invention can be employed.

[0022] The preferred embodiment of the present invention, and a prototype thereof, will now be discussed in detail, making reference to the drawings.

[0023] The basic arrangement of the driving circuit comprises a bipolar transistor to which is applied a control signal for controlling the driving of a light emitting element, and a constant current source for supplying a constant current to the bipolar transistor.

[0024] When an ON signal is applied to the gate of the bipolar transistor, the bipolar transistor is turned on and a current flows between its emitter and its collector. This current, for driving the light emitting element, is supplied from the constant current source.

[0025] In the prototype, discussed in detail below, the driving circuit is a semiconductor integrated circuit having differentially connected bipolar transistors and a MOS transistor on the same substrate, which uses the differentially connected bipolar transistors as a switching circuit, and which has a light emitting element connected to and driven by the bipolar transistor. In this circuit, a constant current circuit using a MOS transistor is connected to the differentially connected bipolar transistors. With this arrangement, it is possible to suppress overshoot and ringing occurring in the driving current of the light emitting element by controlling the response of the constant current source by using a MOS transistor whose mutual inductance is small.

[0026] In use, complementary signals are applied to the bases of the respective differentially connected bipolar transistors. The bipolar transistors, connected to the light emitting element, is switched without being saturated. This allows current switching at the highest speed.

[0027] In the driving circuit of the preferred embodiment, a plurality of MOS transistors are connected in parallel. A MOS transistor such as one formed in the same integrated circuit as bipolar transistors as in the present invention, excluding those fabricated through some special process, such as power MOS transistors, is primarily one of the type used in a logical circuit. Therefore, the current which the MOS transistor can handle is commonly 1 μA or lower. A very large MOS transistor would be necessary to obtain a current of several milliamperes to 100 milliamperes for driving a semiconductor light emitting element. The dimensions of such a MOS transistor obtained by simulation are a gate width of 2000 μm and a gate length of 3 μm. A MOS transistor of this size can no longer be considered as a lumped component, since the current density would vary in the transistor. To prevent this, a plurality of MOS transistors are connected in parallel.

[0028] In addition, a respective time constant circuit, formed in the same integrated circuit as each MOS transistor used as a constant current source, consisting of

a resistor and a capacitor, is connected to the gate of the respective MOS transistor. With this arrangement, the gate potential waveform can be controlled because the time constant is optimised. Consequently, it is possible to obtain a high-speed current waveform free from overshoot and ringing.

[0029] The driving circuit can be realised as a one-chip IC by using well-known IC process techniques. It is also possible to fabricate the circuit by using a compound semiconductor such as gallium arsenide or indium phosphorus. When the driving circuit is fabricated by using the same compound semiconductor as a light emitting element, it is readily possible to integrate the two into one chip.

[0030] Fig. 5 is a circuit diagram showing a prototype semiconductor light emitting element driving circuit. Referring to Fig. 5, npn transistors 1 and 2 are differentially connected. An NMOS transistor 3 has a drain connected to the common emitter of the npn transistors 1 and 2 and operates with a constant current. A semiconductor light emitting element 4 has a cathode connected to the collector of the npn transistor 1 via a parasitic inductance 6 of a line. A resistor 5 as a load is connected to the collector of the npn transistor 2. A parasitic inductance 7 is due to the line between the anode of the semiconductor light emitting element 4 and a power supply 15 as a high-potential reference voltage source. The semiconductor light emitting element 4 has a junction capacitance C_j, 8. The npn transistors 1 and 2 have emitter-collector capacitances 9 and 10, respectively. The NMOS transistor 3 which operates as a constant current source has a drain-gate capacitance 11. One end of a resistor 12 is connected to the gate of the NMOS transistor 3 and to one end of a capacitor 13. The other end of the resistor 12 is connected to the gate and drain of an NMOS transistor 14 for applying a bias potential. The other end of the capacitor 13 is connected to a ground potential 16 as a low-potential reference voltage source. Inverters 17 and 18 supply complementary switching signals to the bases of the differentially connected npn transistors. A constant current source 19 supplies a constant current to the NMOS transistor 14.

[0031] Fig. 6 is a view showing voltage waveforms and current waveforms at individual nodes of the circuit of Fig. 5. The operation of this circuit will be described below with reference to Fig. 6.

[0032] The inverter 17 applies a High-level signal to the base of the npn transistor 1, and the inverter 18 applies a Low-level signal to the base of the npn transistor 2. Consequently, the npn transistor 1 is activated, and the npn transistor 2 is cut off. The collector current of the npn transistor 1, i.e., the driving current of the semiconductor light emitting element changes from 0 to a drain current I of the NMOS transistor 3, which operates with a constant current, after a certain time t. As indicated by (a) and (b) in Fig. 6, the current change I in the time t generates counterelectromotive voltage pulses $L_1 \cdot I/t$ and $L_2 \cdot I/t$ due to the parasitic inductances 6 (= L_1) and 7 (= L_2), respectively. These counterelectromotive voltage pulses are transmitted to the gate of the NMOS transistor 3 through the junction capacitance 8 of the semiconductor light emitting element, the emitter-collector capacitance 9 of the npn transistor 1, and the gate-drain capacitance 11 of the NMOS transistor 3. Potential variations at the emitters of the npn transistors 1 and 2 are illustrated in (e) of Fig. 6, i.e., indicated by the solid-line waveform which is generated by the complementary driving signals to the bases and the dotted-line waveform which is synthesized with the counterelectromotive voltage pulses, respectively. Consequently, the dotted-line potential waveform shown in (f) of Fig. 6 is generated at the gate of the NMOS transistor.

[0033] The mutual conductance, g_m, of the NMOS transistor is represented by

$$g_m = \sqrt{(I_D \cdot \mu_n C_{OX} W/L)}$$

where

I_D : the drain current
μ_n : the mobility of electrons
C_{OX}: the gate capacitance
W : the channel width
L : the channel length

[0034] The above equation demonstrates that the mutual conductance of a MOS transistor is far smaller than that of a bipolar transistor. This indicates that the influence of a potential variation at the gate is small as change in the drain current.

[0035] Furthermore, in this circuit the resistor 12 and the capacitor 13 are connected to the gate of the NMOS transistor 3. Consequently, the behaviour of the gate potential is controlled by a time constant $\tau = C_G \cdot R_G$. That is, the gate potential responds to high-speed pulses with time constant τ.

[0036] Figs. 7A to 7C indicate the driving current waveforms of the semiconductor light emitting element and gate voltage waveforms obtained while changing the time constant obtained by the resistor 12 and the capacitor 13 connected to the gate of the NMOS transistor 3 which operates with a constant current. Figs. 7A to 7C show that when the time constant is made most suitable, a current waveform free from overshoot and ringing can be obtained.

[0037] If the size of a single NMOS transistor is increased to obtain the necessary driving current, the current is distributed and it is not possible to treat the transistor as a lumped component. This makes the optimum design of the circuit difficult.

[0038] In the preferred embodiment of the invention, the single MOS transistor 3 of the prototype is replaced by connecting a plurality of MOS transistors in parallel, which are individually formed in a plurality of active regions formed on an Si substrate and isolated by a field

insulating dielectric film of SiO_2.

(Preferred Embodiment)

[0039] Fig. 8 is a circuit diagram showing a semiconductor light emitting element driving circuit according to the preferred embodiment of the present invention. In this embodiment, a plurality of NMOS transistors 31, 32, 33, ..3n are connected in parallel, and a resistor 41, 42, 43, ..4n and a capacitor 131, 132, 133, ..13n are connected to the gate of each MOS transistor.

[0040] Each MOS transistor is used as a parallel constant current source connected to the emitters of differentially connected bipolar transistors. Additionally, a respective time constant circuit consisting of a resistor and a capacitor is connected to the gate of each MOS transistor. Consequently, with an appropriate choice of time constant, it is possible to obtain a current pulse waveform free from overshoot and ringing.

[0041] Since the semiconductor light emitting element is driven with a stable driving current, the element does not deteriorate. This effectively increases the life of the product.

[0042] Fig. 9 is a sectional view showing a portion of an IC chip in which the driving circuit of the preferred embodiment is formed. In Fig. 9, only one bipolar transistor BPT and two MOS transistors MOS are illustrated, and other components such as a protective layer are omitted. The parts shown in Fig. 9 are a p-type silicon substrate 201, an n^+-type collector buried layer 202, a p-type well 203, an n^--type epitaxial layer 204, a p-type base 205, and an n^+-type emitter 206.

[0043] The two NMOS transistors MOS have sources/drains 207 and 208 and gates 210. A field insulating film 209 isolates the elements.

[0044] A collector line 211 of the bipolar transistor is connected to the terminal of a light emitting element. A base line 212 serves as an input terminal, and a line 213 connects a constant current source to the bipolar transistor. A ground line 214 is connected to a low-potential reference voltage source.

[0045] Fig. 10 is a sectional view showing a portion of an IC chip in which a series circuit of a resistor R and a capacitor C is formed.

[0046] In this series circuit in Fig. 10, n^+-type diffusion layers 221 and 222 are formed, and a series connecting line 215 connects the resistor R and the capacitor C. The circuit also includes an insulating interlayer 230.

[0047] The driving circuit is formed into a single chip as illustrated in Fig. 9 by a fabrication method called a BiMOS process or a BiCMOS process. The series circuit shown in Fig. 10 is also monolithically integrated with the driving circuit.

[0048] Figs. 11A and 11B illustrate examples of systems using the circuit of the present invention. Fig. 11A shows a printer, and Fig. 11B shows an optical communication system.

[0049] The printer shown in Fig. 11A comprises a photosensitive drum DRM, a cleaner CLN, a charger CGR, and an exposure unit EXP which employs the driving circuit of the present invention, a developing unit DVLP, and a recording medium P.

[0050] The exposure unit EXP uses an LED array or a laser diode as a light emitting element and forms latent images on the photosensitive drum by using light from the light emitting element.

[0051] In the communication system shown in Fig. 11B, the transmission side includes a laser diode LD as a light emitting element and a transmitter SYS1 with a driving circuit, and the reception side includes a photodiode sensor PHD and a receiver SYS2.

[0052] An optical fibre OFR also is provided.

[0053] The light emitting element driving circuit is adopted in the transmitter SYS1.

Claims

1. A driving circuit for driving a light emitting element, which circuit is an integrated circuit comprising:

   a constant current source (3) including an FET drive transistor (31); and
   a pair of bipolar transistors (1,2), the emitters of which are connected to said constant current source, to provide a constant-current differential switch for controlling and driving the light emitting element (4) connected to and driven by a collector of one of said bipolar transistors (1,2):

   characterised in that:

   said constant current source (3) is formed of a plurality of MOS FET drive transistors (31,32,..) which are connected in parallel and have their drains connected to the emitters of said bipolar transistors (1,2), each of said MOS FET transistors having, connected to its gate electrode, a respective time constant circuit consisting of a resistor (41,42,...) and a capacitor (131,132,...).

2. A circuit according to claim 1 wherein each one of said MOS transistors (31,32...) is formed separately on an active region (203) separated by a field insulating film (209) of SiO_2 on a Si substrate (201).

3. A circuit according to claim 1 incorporated on the same substrate (201) as, and integrated with, the light emitting element (4).

Patentansprüche

1. Treiberschaltung zur Ansteuerung eines lichtemit-

tierenden Elementes, wobei die Schaltung eine integrierte Schaltung ist, mit

einer Konstantstromquelle (3) mit einem FET-Treibertransistor (31), und
einem Paar Bipolartransistoren (1,2), deren Emitteranschlüsse an die Konstantstromquelle angeschlossen sind, um einen Konstantstrom-Differenzschalter zur Steuerung und zur Ansteuerung des an einen Kollektoranschluß von einem der Bipolartransistoren (1, 2) angeschlossenen und durch diesen angesteuerten lichtemittierenden Elementes (4) bereitzustellen,

dadurch gekennzeichnet, daß

die Konstantstromquelle (3) aus einer Vielzahl von parallel geschalteten MOS-FET-Treibertransistoren (31, 32, ...) besteht, deren Drainanschlüsse an den Emitteranschlüssen der Bipolartransistoren (1, 2) angeschlossen sind, wobei jeder der MOS-FET-Transistoren eine an dessen Gateelektrode angeschlossene jeweilige Zeitkonstantenschaltung aus einem Widerstand (41, 42, ...) und einem Kondensator (131, 132, ...) aufweist.

2. Schaltung nach Anspruch 1, wobei jeder der MOS-Transistoren (31, 32, ...) einzeln auf einem durch einen feldisolierenden SiO2 Film (209) getrennten aktiven Bereich (203) auf einem Si Substrat (201) gebildet ist.

3. Schaltung nach Anspruch 1, die auf dem selben Substrat (201) wie das lichtemittierende Element (4) und mit diesem integriert ausgebildet ist.

Revendications

1. Circuit d'attaque pour attaquer un élément émetteur de lumière, ce circuit étant un circuit intégré comprenant :

une source de courant constant (3) comprenant un transistor d'attaque constitué d'un transistor à effet de champ (31) ; et
une paire de transistors bipolaires (1, 2) dont les émetteurs sont connectés à ladite source de courant constant, de façon à constituer un commutateur différentiel de courant constant pour commander et attaquer l'élément émetteur de lumière (4), connecté à un collecteur de l'un desdits transistors bipolaires (1, 2) et attaqué par celui-ci ;

caractérisé en ce que :

ladite source de courant constant (3) est formée d'une pluralité de transistors d'attaque constitués de transistors à effet de champ métal-oxyde-semiconducteur (MOSFET) (31, 32, ...) qui sont connectés en parallèle et ont leurs drains connectés aux émetteurs desdits transistors bipolaires (1, 2), chacun desdits transistors à effet de champ métal-oxyde-semiconducteur ayant, connecté à son électrode de grille, un circuit de constante de temps respectif composé d'une résistance (41, 42, ...) et d'un condensateur (131, 132, ...).

2. Circuit selon la revendication 1, dans lequel chacun desdits transistors métal-oxyde-semiconducteur (31, 32, ...) est formé séparément sur une région active (203) séparée par un film d'isolement de champ (209) en SiO_2 sur un substrat de Si (201).

3. Circuit selon la revendication 1, incorporé sur le même substrat (201) que l'élément émetteur de lumière (4), et intégré à celui-ci.

FIG. 1

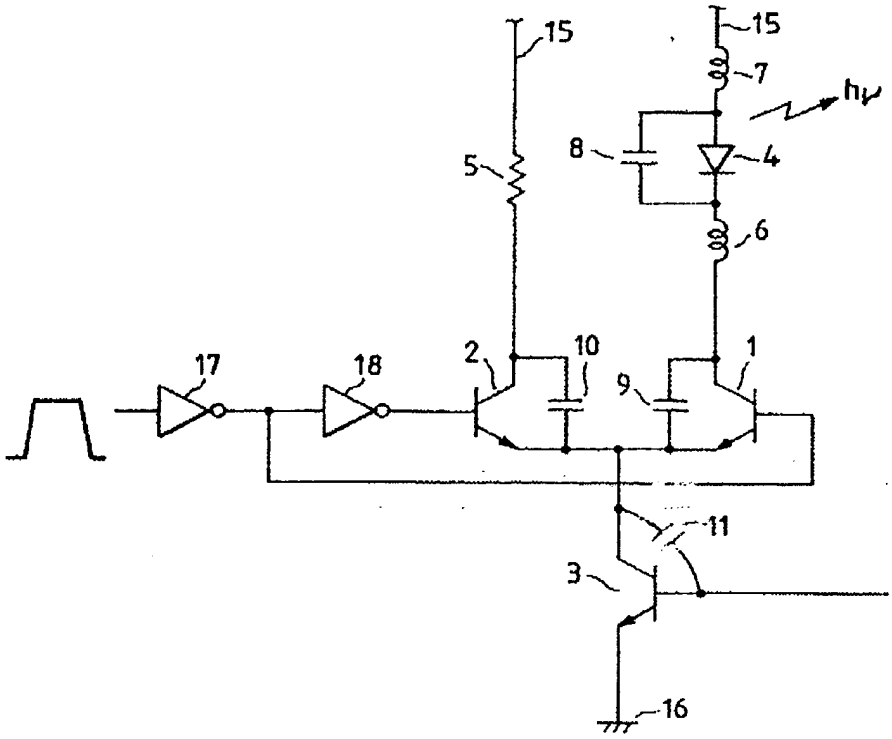


FIG. 2

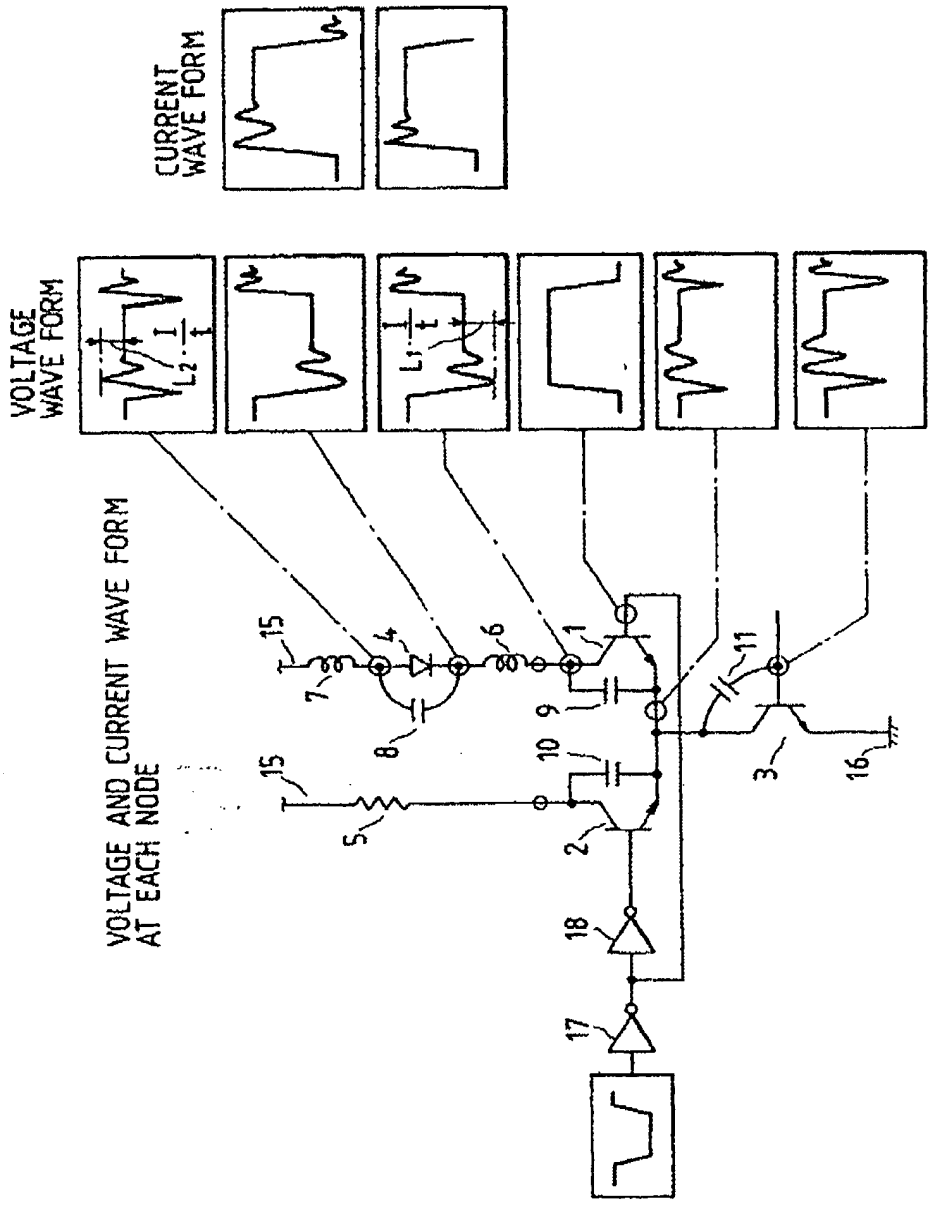

CURRENT WAVE FORM
VOLTAGE WAVE FORM
VOLTAGE AND CURRENT WAVE FORM AT EACH NODE
15
7
4
6
1
8
9
11
10
15
5
2
3
16
18
17

FIG. 3

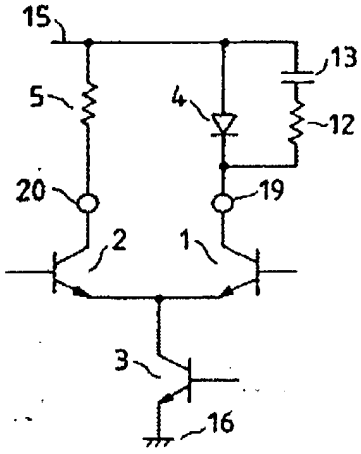


FIG. 4

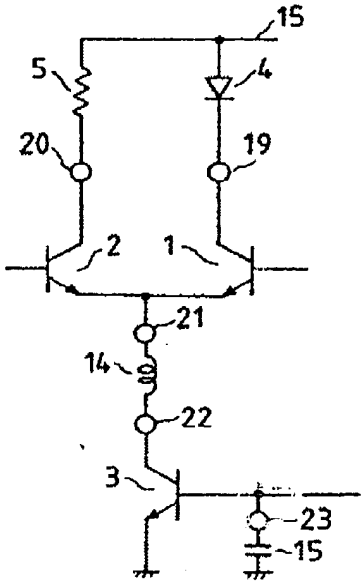


FIG. 5

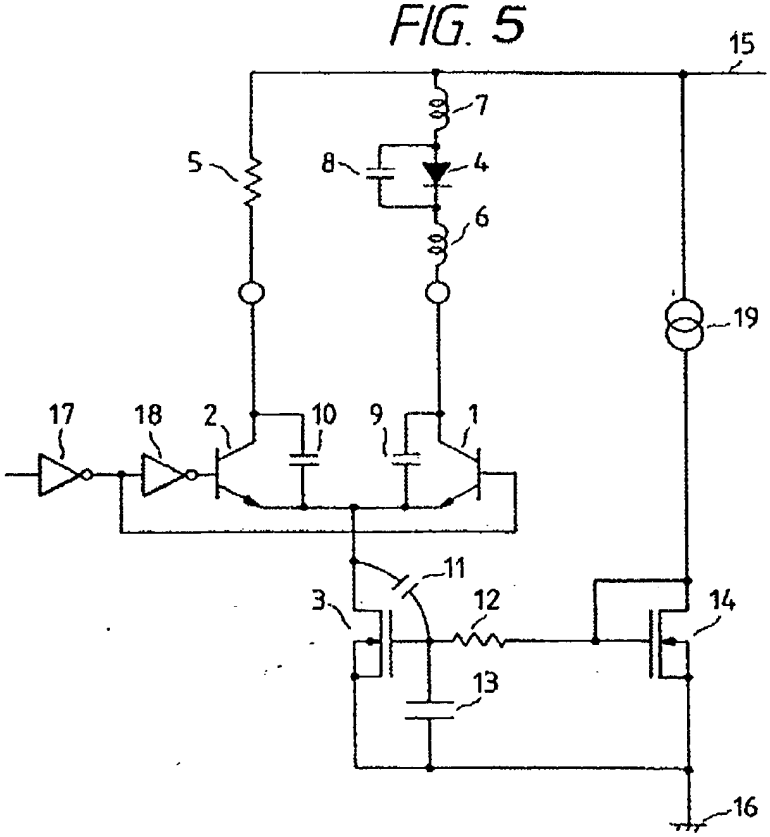


FIG. 6

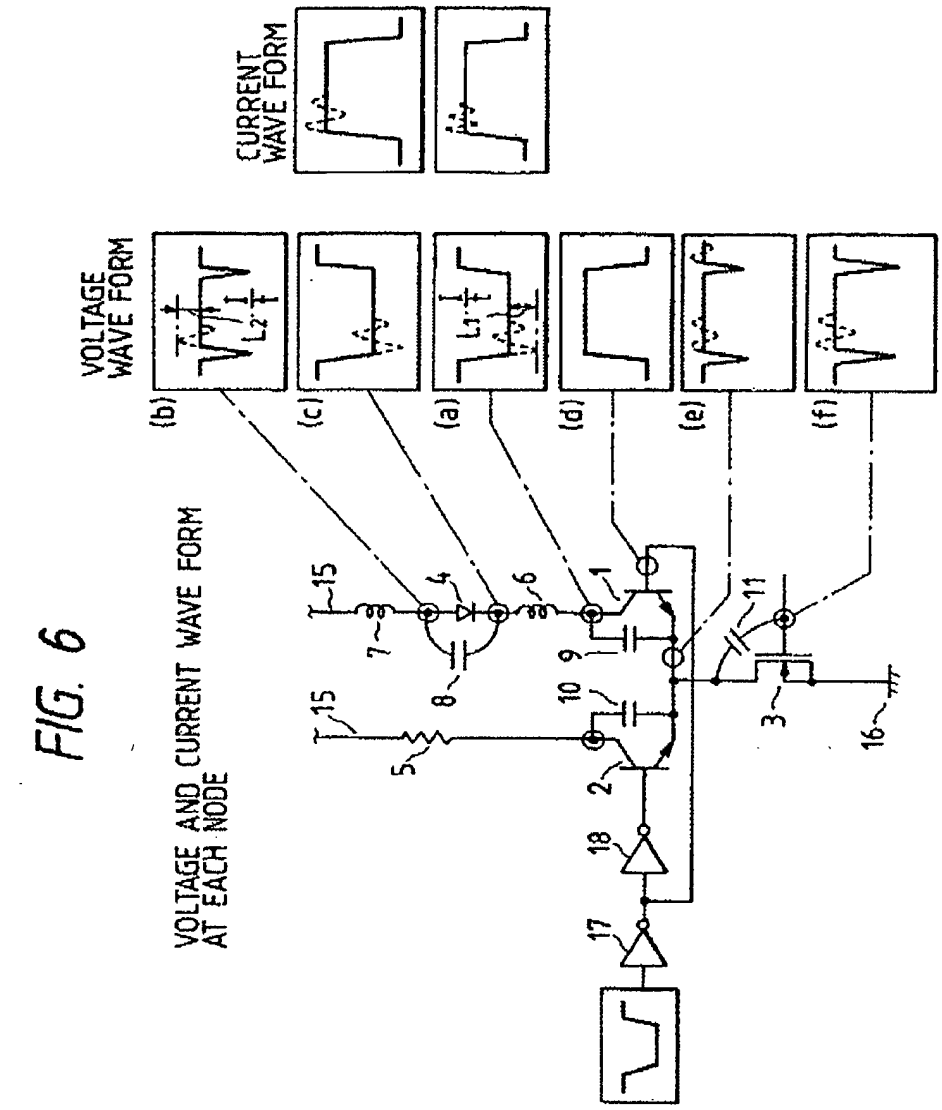

VOLTAGE AND CURRENT WAVE FORM AT EACH NODE
VOLTAGE WAVE FORM
CURRENT WAVE FORM
(b)
(c)
(a)
(d)
(e)
(f)
L2
L1
15
4
6
1
7
8
9
10
11
5
2
3
16
18
17

FIG. 7C

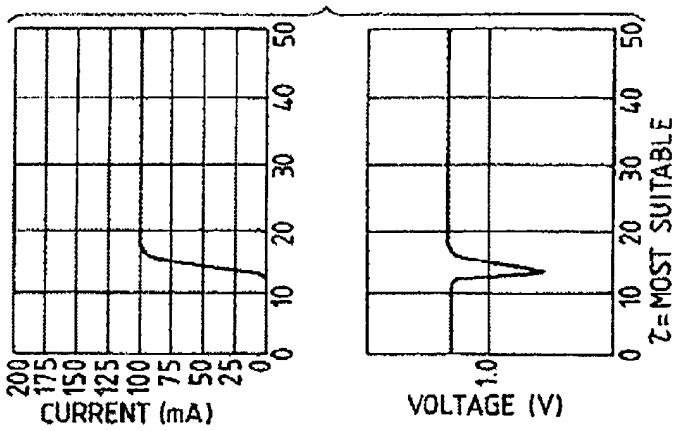


FIG. 7B

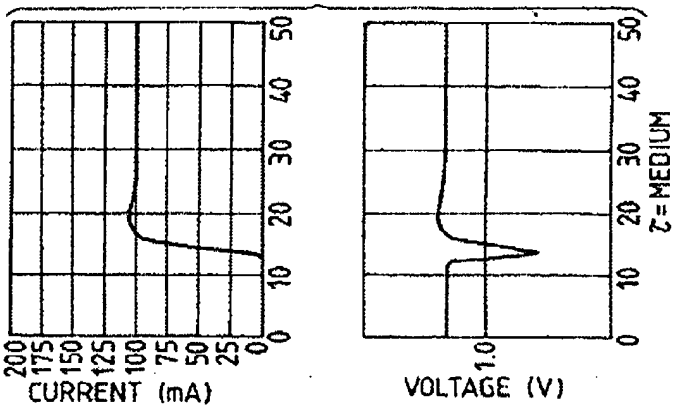
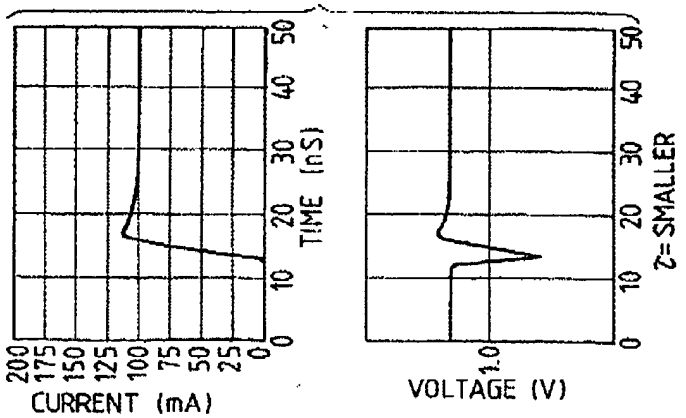


FIG. 7A



SEMICONDUCTOR LIGHT EMITTING ELEMENT DRIVING CURRENT WAVE FORM (UPPER)
CONSTANT CURRENT NMOS GATE VOLTAGE WAVE FORM (LOWER)

FIG. 8

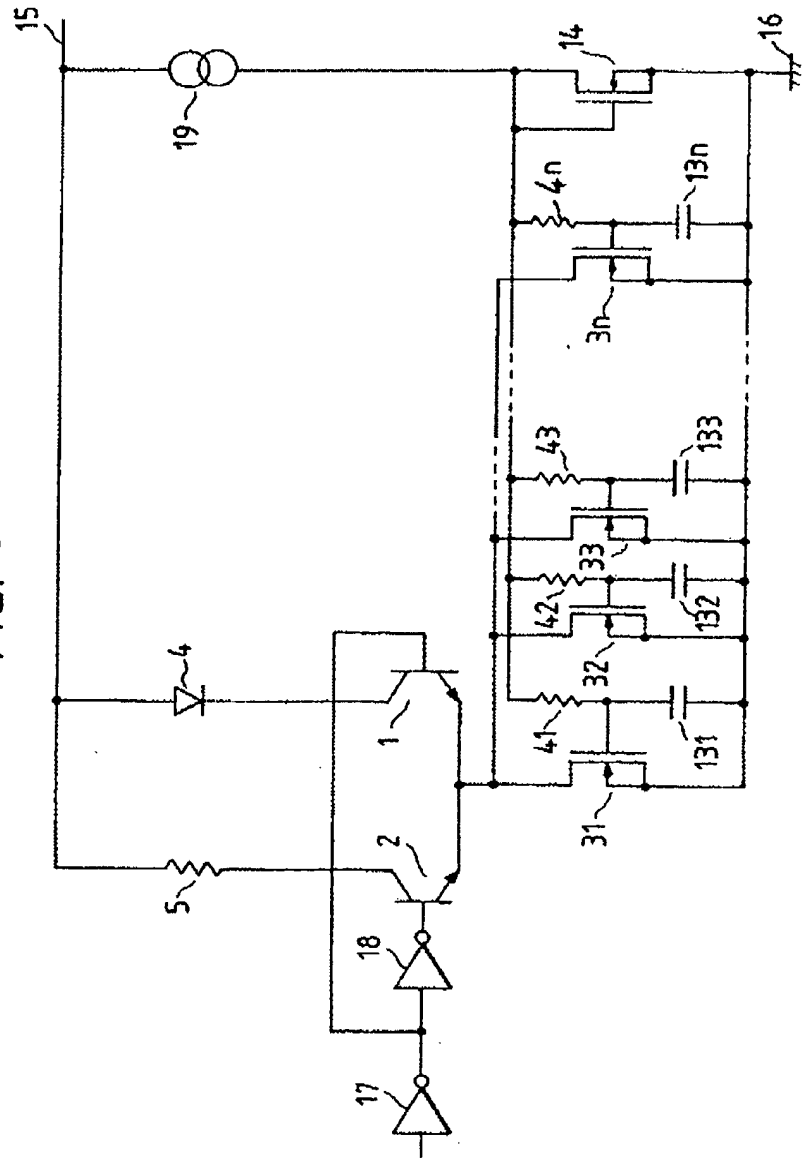


FIG. 9

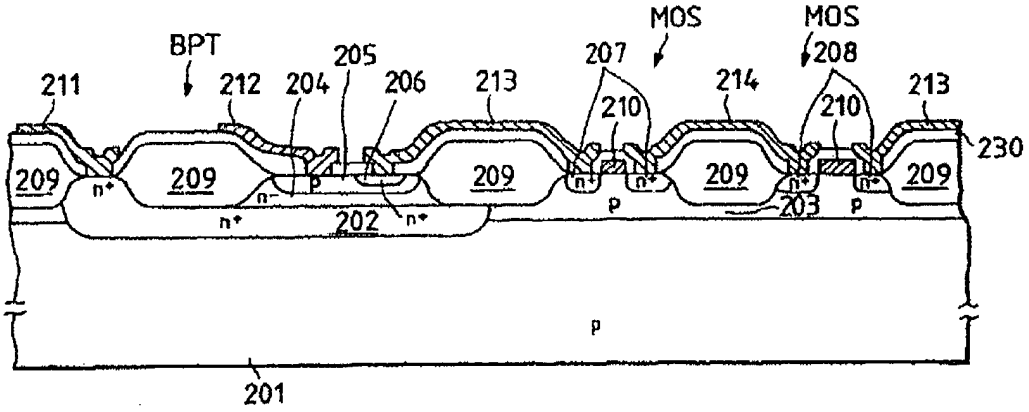


FIG. 10

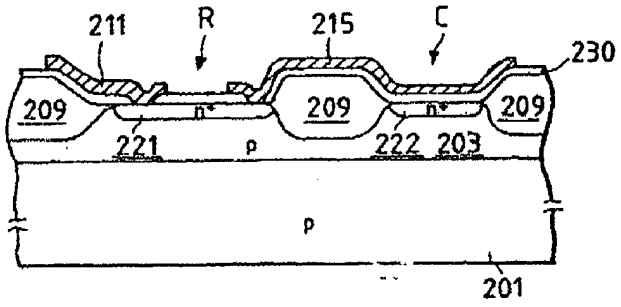


FIG. 11A

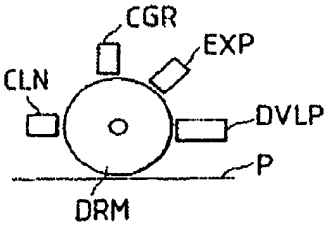


FIG. 11B